



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit 2154

Examiner Larry Donaghue

In Re: Mario Nemirovsky et al.
Case: P3803
Serial No.: 09/312,302
Filed: 05/14/1999
Subject: Interrupt and Exception Handling for Multi-Streaming Digital Processors

To: The Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Dear Sir:

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Enclosed herewith is an Information Disclosure Statement (IDS) by Applicant listing seventeen (17) references. As required under §1.98(d) copies of references are enclosed. Applicant desires that the references be entered in the above referenced case as relevance dictates.

As this IDS is filed before the mailing of a first Office action after the filing of a request for continued examination, no fee for the IDS is required, in accordance with rule 1.97. Please charge any additional fees required or credit any overpayment to Deposit Account No. 50-0534.

Respectfully submitted,
Mario Nemirovsky et al.
by

Donald R. Boys
Reg. No. 35,074

Central Coast Patent Agency, Inc.
P.O. Box 187
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First Named Inventor: Mario Nemirovsky

Serial Number: 09/312,302

Filing Date: 05/14/1999

Title of Case: Interrupt and Exception Handling for Multi-Streaming Digital Processors

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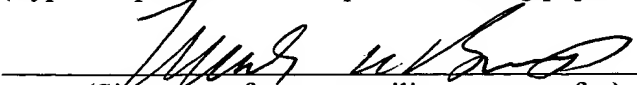
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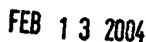
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1. Information Disclosure Statement.
2. Cover Letter for Information Disclosure Statement.
3. Copies of seventeen (17) publications cited in the IDS.
4. Certificate of express mailing.
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Mark A. Boys

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Application Number	09/312,302
Filing Date	05/14/1999
First Named Inventor	Mario Nemirovsky
Art Unit	2154
Examiner Name	Larry Donaghue
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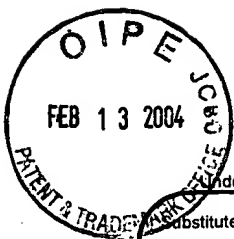
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STATEMENT BY APPLICANT**

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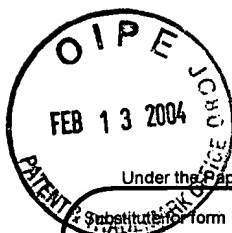
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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan Kaufmann, San Francisco	
		MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
		POTEL, M.J., Real-Time Playback in Animation Systems, Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp. 72-77, San Jose, CA	
		ARM Architecture Reference Manual, 1996, pp. 3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall	
		ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at : http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS)	
		MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp. 10-66, 10-67 and 10-71, Motorola, Inc.	
		DIEFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, pp.40-63, Vol. 12, No. 2	
		KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp 7-106 and 7-107, Prentice Hall, New Jersey	
		DIEFENDORFF, KEITH et al., AltiVec Extension to PowerPC Accelerates Media Processing, March - April 2000, pp. 85-95, IEEE Micro, Vol. 20, No. 2	
		PAI, VIJAY et al., An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors, Proceedings of ASPLOS-VII, October 1996, pp. 12-23, ACM, Inc.,	

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		GRUNEWALD, WINFRIED et al., Towards Extremely Fast Context Switching in a Block-Multithreaded Processor, Proceedings of EUROMICRO-22, 1996, pp. 592-599	
		BRADFORD, JEFFREY et al., Efficient Synchronization for Multithreaded Processors, Workshop on Multithreaded Execution, Architecture and Compilation, January-February 1998, pp. 1-4	
		TULLSEN, DEAN et al., Supporting Fine-Grained Synchronization on a Simultaneous Multithreading Processor, UCSD CSE Technical Report CS98-587, June 1998, all pages, US	

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